Increasing the Conversion Speed of the Counter-Ramp Analog-to-Digital Converter Based on Starting with Suitable Count

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Abstract: In this paper, a proposed technique is designed and implemented for increasing the conversion speed of the Counter-Ramp A/D converter. It depends on starting with suitable count, whereas, the ordinary Counter-Ramp type always starts from zero (0) count in each conversion process. In this work, four starting count points is proposed ($(00)_H$, $(40)_H$, $(80)_H$, and $(C0)_H$). For very low level analog input signal, the proposed A/D converter starts from $(00)_H$, and for higher level of input signal the proposed circuit starts from $(40)_H$, and for high input signal level it will start from $(80)_H$ or $(C0)_H$ depending on signal level value. Increasing these starting counts leads to increase in the conversion speed more and more, but at same time, more analog comparators should be added to the proposed circuit, i.e. the complexity of the circuit will be increased. The proposed circuit is tested practically using 16 and 32 levels of analog input signal, and the results are stimulating. The maximum conversion time value is lower than that of ordinary Counter-Ramp type, where, for the proposed circuit is close to 0.640 µsec, while for ordinary Counter-ramp type its value is close to 2.56 µsec.

Keywords: A/D Converter, Conversion Time, Programmable Binary Counter, Proper Address Producer, Starting Count.

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1. Introduction

The Analog-to-Digital Converter is a device used for converting the analog (or continuous) signal comes from analog transducers such as microphone or any sensor of environmental conditions to digital (or discrete) signal, whereas, a level of analog signal can be translated to a group of binary numbers (bits). The A/D converter is considered as an interface or adapter between the analog and digital systems.

Generally, for most environment sensing applications, the analog signal of the sensors, must be converted to digital form, because the digital signals can be easily processed using Digital Signal Processors DSPs. Most types of A/D converters have comparator circuit in their circuit designs. This comparator compares the analog input signal with reference signal, and the output signal of this comparator is a logic state, (1) or (0). The logic (1) state will be presented if the reference signal is equal or larger than the analog input signal, and (0) state will be presented if the reference signal is lower than the input signal. The comparator circuit is the fundamental element of the A/D converter circuit, which translates the comparison between the analog input and reference signals to digital decision [1].

The Counter-Ramp A/D converter consists of the following parts: clock generator, AND gate, analog comparator, D/A converter, and binary counter. Figure 1 illustrates one of models of this type of Converter [2].

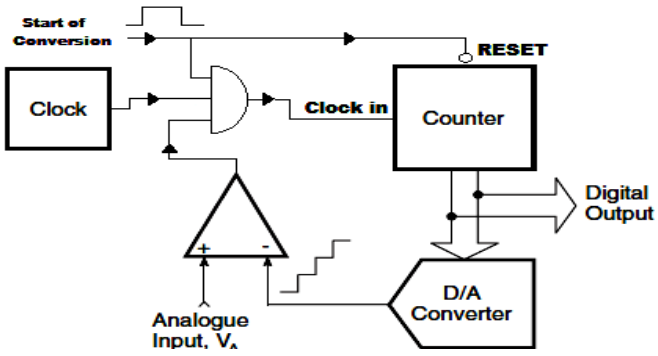

Figure 1. The Circuit Diagram of the Counter-Ramp A/D Converter.

At the beginning of the conversion process, the output of the binary counter is at RESET state $(0)_H$, and the output of the Analog Comparator is at HIGH state. Now when a HIGH state is applied to input of the Start of Conversion, the AND is activated and the output clock pulses is entered to the clock input of the binary counter. At this time the counter will count the incoming pulses, at the same time the D/A converter converts the digital output of the binary counter to an analog signal that is used as a reference signal which is fed to the inverting input of the analog comparator, while the non-inverting input of this comparator is fed by the analog input signal V_A that must be converted to binary data. The binary counter will continue to count the incoming pulses from the clock generator until it reaches to a specific count (binary number) where the output of the comparator is changed to LOW level and the AND gate will be deactivated, and this change is occurred due to the fact that the reference signal at the inverting input of the Comparator will be more than the analog input signal. The last count will represent the digital form of the analog input signal. When the state of the conversion starting input is suddenly changed from HIGH to LOW the binary counter will be at RESET state and the conversion process has finished at this moment. As at each conversion process the binary counter will starts from zero count $(0)_H$, and due to this reason the Counter-Ramp type is slow in its process of conversion at high values of analog input signals [2].

The proposed technique consists of four main parts: proper address producer, EPROM (Erasable Programmable Read Only Memory), programmable binary counter, and latch. The role of the first part is to produce a proper address to the second stage (EPROM) according to analog input level. This stage consists of several comparator circuits, which are arranged according to the threshold (reference) voltage levels. By increasing the number of these comparators, a reduction in the maximum conversion time is obtained. The role of the second part is to produce a proper data of starting count according to the applied address from the first part. The third part is the 8-bits programmable binary counter, which is used for counting the output pulses of the 100 MHz crystal oscillator for a period of time depending on the input voltage level. The fourth part is the latch circuit, which is used for holding the corresponding count of the input voltage value at the end of every conversion process.

2. Related Works

In 2015, J. Pickering [3] had presents a method of improving the Counter-Ramp A/D converter circuit by reducing its conversion time, which is the essential element of A/D converters. It had used a method of pursuit the input analog voltage at every conversion process. The difference between this method and the traditional Counter-Ramp type is the using of up-down counter that counts up or down depending on logic state of output of an analog comparator, whereas, this comparator compares the analog input voltage with the output of a Digital-to-Analog D/A converter, the digital input of this D/A converter is connected to the output of the up-down binary counter. In this method the binary counter does not start from zero count as in traditional Counter-Ramp A/D converters, but it starts from the last reading count , and then the counter will count up or down according to the state of the analog comparator, so, the proposed technique in this work is faster than the classical Counter-Ramp A/D converter.

In 2015, B. Verbruggen [4] had presents a number of different types of high speed A/D converters. One of these A/D converters is the ultra-speed Counter-Ramp type. In this converter type, the conversion speed has been increased by increasing the output frequency value of the local oscillator, which reduces the conversion time to tens of nanoseconds. This A/D converter has used ultra-speed components such as ultra-high speed analog comparators and CMOS digital integrated circuits ICs. The output frequency value of local oscillator of this ultra-speed A/D converter had reached to 1 GHz. Good results has been obtained by testing this A/D converter for many measurement reading of analog input signal in the range (0-5) Volts.

In 2017, Y. Duan [5] has presented a proposed technique of increasing the conversion speed (i.e. reducing the conversion time) of the Counter-Ramp A/D converter circuit that used in high speed data communication. This technique depends on the level of the analog input voltage, for more than mid value of full scale input voltage, the proposed circuit will start from zero value, then the binary counter will count down until it reaches to the proper binary count data, while for less than mid value of full scale input voltage the proposed circuit will starts from zero and the binary counter will count up until it reaches to the proper output binary data. The binary counter of this A/D converter circuit always starts from zero count at

every conversion process. In this proposed circuit, a high speed local frequency generator has been utilized that have frequency 1.7 GHz, and also a high speed analog comparator and high speed CMOS logic integrated circuit has been used to make the conversion time to reduce to a few of nanoseconds, which is a stimulant result.

3. Principle of Proposed A/D Circuit

The block diagram of the proposed circuit has been illustrated in Figure 2. As shown, it consists of seven stages: proper address producer, EPROM, crystal oscillator, programmable binary counter, D/A converter, latch, and control circuit.

When the analog input voltage is applied to the input of the proposed circuit, the proper address producer presents a proper address to the address lines of the EPROM IC according to the level of the applied analog signal. The EPROM IC presents a proper count data that will be applied to the data input of the programmable binary counter.

The conversion process begins when a pulse is applied to the input of the start of conversion. At this moment and according to the level of the D/A converter that is lower than or equal to the input voltage, the control unit instructs the programmable binary counter to start to count the incoming pulses from the output of the crystal oscillator depending on the start count data that is presented from the EPROM IC. This process continues until the output of the D/A converter reaches to the analog input level. At this moment, the control unit instructs the Binary Counter to stop the counting process, and then it instructs the Latch IC to hold the final count of the binary counter. This final count of the binary counter represents the binary data that corresponds to the analog input voltage. The Control Unit instructs binary counter to stop the counting process depending on a comparator circuit that is included in it, this comparator compares the applied analog signal with the output analog signal of the D/A converter circuit.

It is clear that, at every conversion process, the binary counter starts to count from a suitable count data and that leads to get the proper count corresponds to the applied analog input voltage, while the counter-ramp converter type starts from zero count at each conversion process, then

one can conclude that the proposed A/D converter is so faster than the counter-ramp type.

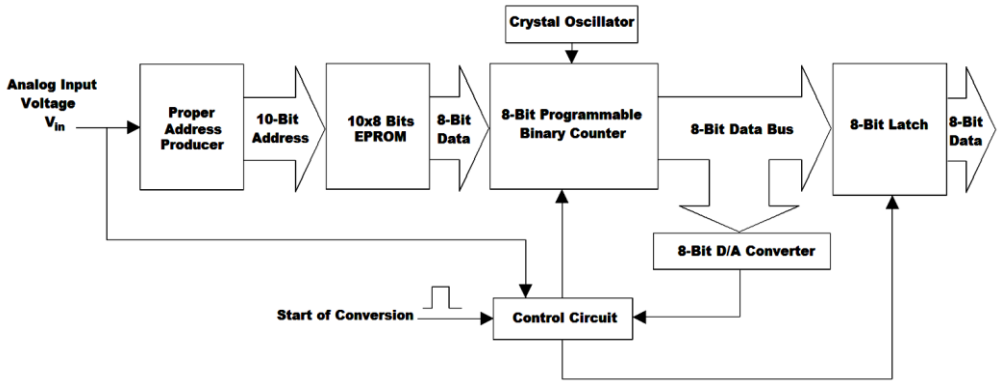

Figure 2. Block Diagram of the Proposed Circuit.

4. Proposed Circuit Details

The circuit diagram of the proposed system is shown in Figure 3. As illustrated, the analog input signal must be applied to the input of the proper address producer, which is constructed from the four comparator integrated circuits IC1, IC2, IC3, and IC4 (the type of these comparators is IC LM393) [6]. Four starting count data is proposed for this system and then four threshold levels should be proposed for these comparators, which are: 0.8, 0.6, 0.4, 0.2 Volt, which corresponds to starting count data $C0_H$, 80_H, 40_H, 00_H. IC1 has a threshold of 0.8 Volt, IC2 has threshold of 0.6 volt, IC3 has threshold of 0.4 Volt, and IC4 has threshold of 0.2 Volt. This unit presents four address lines A_0, A_1, A_2, and A_3 to the address input of the EPROM IC7 (the type of this memory unit is 2708) which it has a size 8K bits [7]. This EPROM saves the selected starting count data according to Table 1.

The Crystal Oscillator of this system is composed from three Inverters IC12, 100 MHz Crystal, and several resistors and capacitors. This oscillator presents clock pulses to the clock input of the programmable binary counter IC8 and IC9 such the fully count from 00_H to FF_H. The frequency of this oscillator is 100 MHz. The Programmable Binary Counter

is composed from two 4-bit of programmable binary counter IC8 and IC9 (type SN74ALS163) [8].

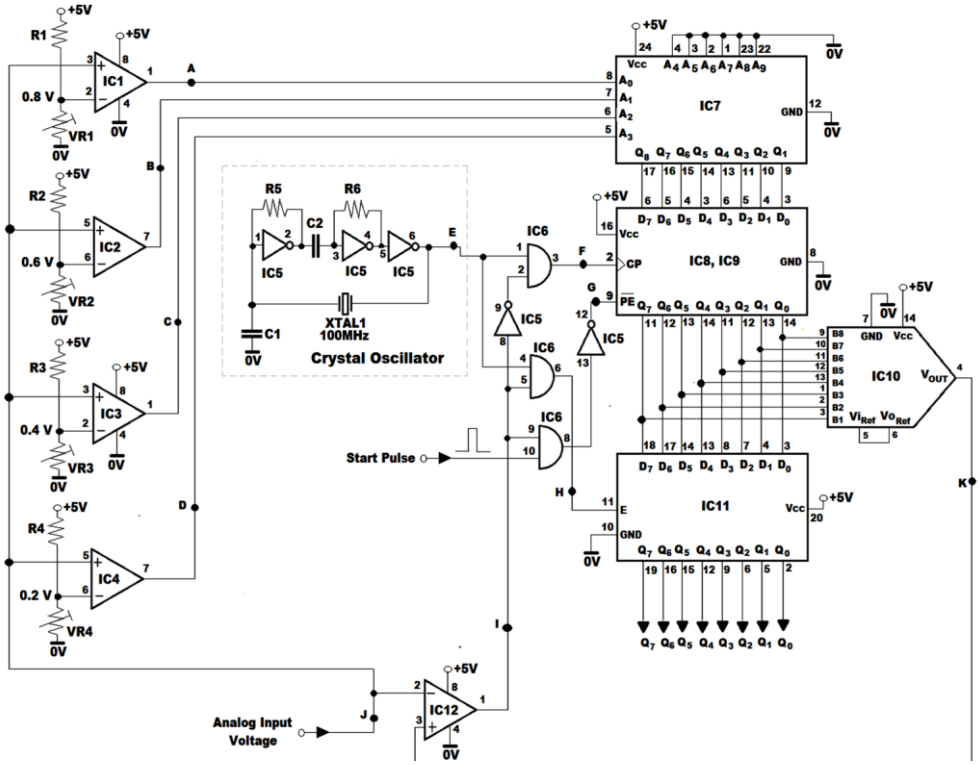

Figure 3. Circuit Diagram of the Proposed A/D Converter Circuit.

Table 1: Address and count data bits of the EPROM IC7.

Address Bits										Data Bits							
A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1

The starting count data of this binary counter is loaded from the EPROM IC7 according to a signal presented by the inverter IC5 (type SN74ALS04) (one of components of the control unit), this signal is applied to the pin9 (PE) of the binary counter.

The 8-Bit output data of the binary counter is applied to the 8-input lines of the D/A converter IC10 (type ZN426) [9] and the output of this converter has been connected to the non-inverting input of the Comparator IC12 (type LM393), while the inverting input of this comparator is connected to the analog signal input. The comparator IC12 presents LOW level when the output of the D/A converter is lower than the analog input signal, and presents HIGH level when the output of the D/A converter equals or exceeds the analog input voltage.

The 8-bit Latch IC11 (type SN74ALS373) [7] is used for holding the output data of the programmable binary counter IC8 and IC9 according to a signal produced from the AND gate IC6 (type SN74ALS08) [7], which is one of components of the control unit. The holding process is achieved at the end of conversion process.

The state transition diagram of the proposed circuit has been shown in Figure (4), which displays the state transition of the fundamental signals generated in the proposed circuit. This state diagram represents the conversion of an analog input voltage of 7.81×10^{-3} Volt, which has been converted to binary number $(00000010)_2$ or 02_H.

The process is started when a 7.81×10^{-3} Volt is applied to the input of the proposed circuit. At this moment, the output of the proper address producer (A_0 A_1 A_2 and A_3) will be (0001), which is presented at points (A B C and D). Then the EPROM IC7 will generate $(00000000)_2$ binary data according to Table 1. Then this data is loaded to the output of the binary counter by applying the start pulse to the input of start of conversion of the proposed circuit and then the counter will start from the count $(00000000)_2$ and continues to count until $(00000010)_2$ count. This count represents the binary data that corresponds to the input voltage. At this moment, the output value of the D/A converter IC10 reached to 7.81×10^{-3} Volt, and then the comparator IC12 will give HIGH at its output, which is used to stop the counting of the binary counter. The last count is loaded to

the output of the Latch IC11 according to a signal that is applied to Enable pin of the latch IC (pin11).

5. Results and Discussion

The theoretical results of the proposed A/D converter circuit are illustrated in Figure 4. These results represent the relation between the analog input voltage and the output number in decimal form. This figure shows the variation of the input voltage in the range from 0 to 1, and the output decimal number in the range from 0 to 255. From Figure 4, the input voltage is linearly increasing with increasing the output number, and this relation is considered a characteristic of one bit conversion steps (256 quantization steps) for the proposed A/D converter (with 8-bit Resolution).

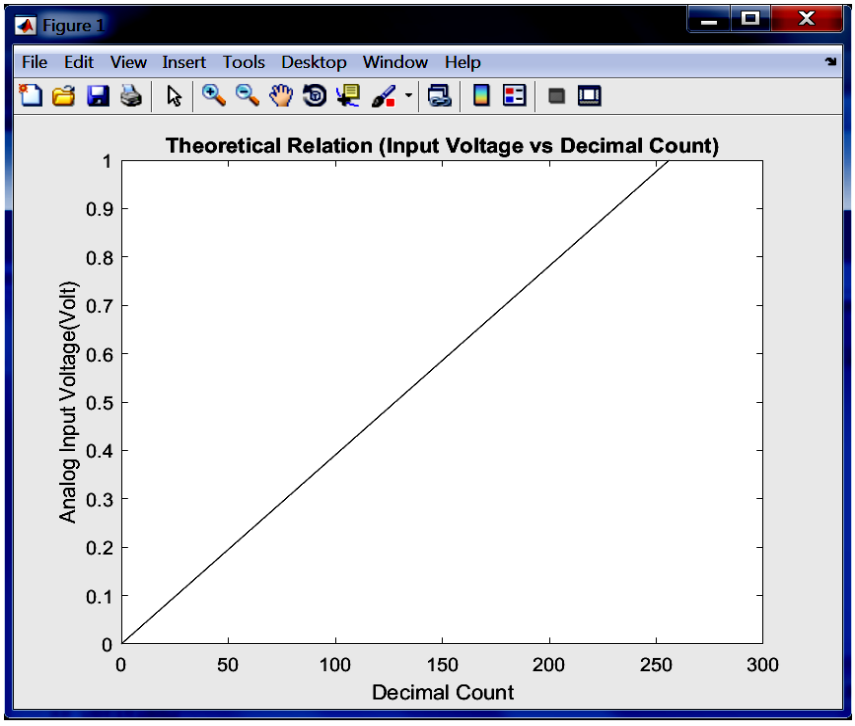

Figure 4. Theoretical Results of the Proposed A/D Converter Circuit.

The practical results of the proposed circuit is shown in Figure 4, it represents the relation between the analog input voltage and the output count data in decimal form. This relation is presented according to Table 2 by testing the proposed circuit at 16 quantization steps. As shown from Table 2, the analog input voltage is varied in the range from 0 to 0.93 Volt at 16 steps, while the output count had varied in the range (00000000-11110000)$_2$.

Table 2: The practical output data related to the input voltage readings.

Analog Input Voltage	Digital Output	
	Binary Form	Decimal Form
0	00000000	0
0.06	00010000	16
0.12	00100000	32
0.18	00110000	48
0.25	01000000	64
0.31	01010000	80
0.37	01100000	96
0.43	01110000	112
0.5	10000000	128
0.56	10010000	144
0.62	10100000	160
0.68	10110000	176
0.75	11000000	192
0.81	11010000	208
0.87	11100000	224
0.93	11110000	240

As illustrated in Figure 5, the resultant relation line is linear with existence of some slight fluctuations (i.e. not pure line). These fluctuations occurred due to using of the quantization process for the analog input voltage. The quantization means that the analog input voltage is divided to number of voltage levels (steps), i.e. the proposed circuit does not deal with continuous input voltage. Therefore, the proposed A/D converter circuit will deal with discrete input voltage levels, and there is range of voltage values between the quantization voltage steps, where, the proposed circuit does not respond to variation in these voltage ranges. Always, all the A/D converter types suffer from this problem (non-linearity), which causes some fluctuations in the linear relation between the analog input voltage and the output count (data).

One can observe the similarity between the theoretical and practical results shown in Figures 4 and 5, which supports the success of design and performance of the proposed circuit for 16 practical reading samples.

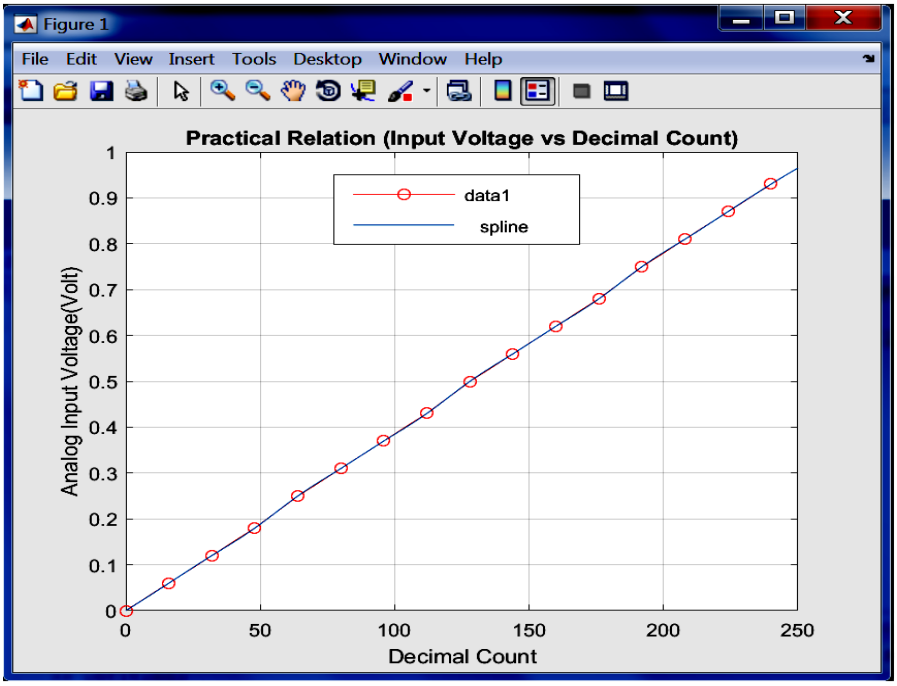

Figure 5. Practical Results of the Proposed A/D Converter Circuit with 16 measurement points.

Another practical result is presented in Figure 6, which represents the relation between the analog input voltage and the decimal representation of the output digital data. The relation is plotted by testing the proposed circuit with 32 measurement points. The analog input voltage in the range of 0 to 0.93 Volt and the decimal representation of output digital data in the range of 0 to 248. As shown in this figure, the relation is pure linear with existence of several deviations in the curve line, these deviations is occurred due to using of the quantization process for the analog input voltage. In figure 6, the analog input voltage step is 0.06 Volt, while the decimal output data step is 8. The resultant relation of Figure 6 has supported the successfulness of the design and concept of the proposed circuit.

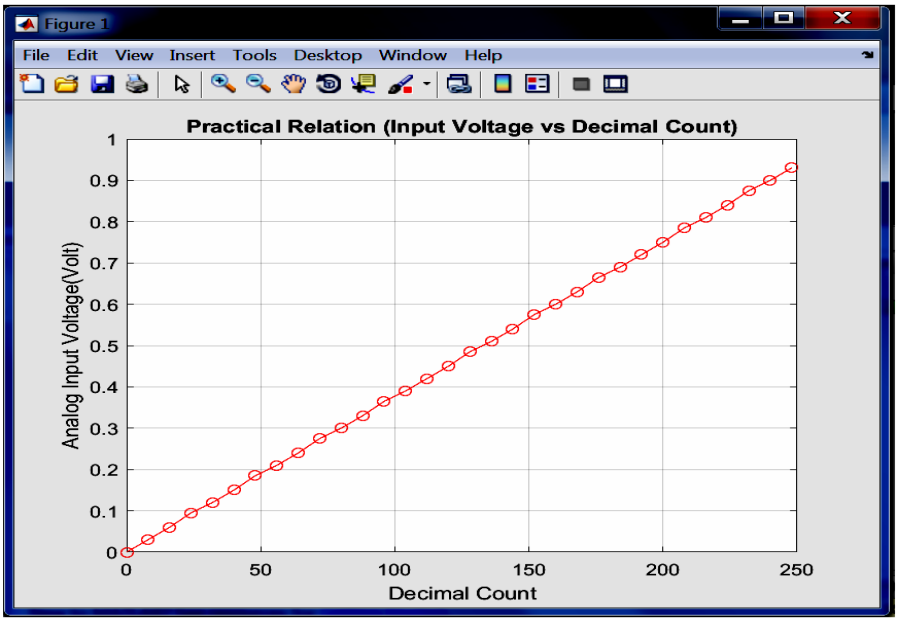

Figure 6. The relation between the analog input voltage and decimal representation of digital output data with 32 measurement points.

The main characteristics of the proposed circuit are presented in Table 3. In this paper, the most important characteristic was the Maximum Conversion Time, which is considered a contribution for this work. As shown, it is 640nsec, while the estimated value of this characteristic is 2.56 µsec for counter-ramp type A/D converter with the same Resolution and clock frequency. Therefore, one can conclude that the maximum conversion time of the proposed circuit is less four times from that of the traditional counter-amp type.

Table 3: The main characteristics of the proposed A/D converter.

Main characteristics	Value
minimum conversion time	10 nsec
maximum conversion ime	640 nsec
digital resolution	8-bit
voltage resolution	0.0039 Volt
accuracy	0.39%

6. Co[illegible]

The proposed A/D converter circuit is considered an improved Counter-Ramp A/D converter type. It solves the problem of long duration of

maximum conversion time of the last type, and therefore, it can reduce this time to an acceptable value to increase the conversion speed more and more. This technique is considered a composition between the Flash and Counter-Ramp types of A/D conversion techniques.

The proposed technique is used the principle of starting with a proper count, where the value of this count depends on the input signal level.

Several analog comparators are utilized in the proposed circuit. These comparators are related to the corresponding proper starting counts of the conversion process. Then the complexity and cost of the proposed circuit will be more than that of counter-ramp converter type.

The Maximum Conversion Time of the proposed circuit can be reduced more and more by adding further comparators in the stage of proper address producer, but this operation will increase the complexity and cost of the proposed circuit.

The conversion speed of the proposed A/D converter circuit depends upon the propagation delay of the used components (especially the EPROM IC) and the frequency of the crystal oscillator, and then it can be increased by using fast ICs, and by increasing the frequency of the crystal oscillator.

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زيادة سرعة التغيير لمحول الإشارة التماثلية الى رقمية من نوع عداد-منحدر بالاعتماد على البدء بِعَدّ مناسب

م. د. أزاد بدر سعيد*

المستخلص: في هذا البحث تم تصميم و بناء تقنية مقترحة لزيادة سرعة التحويل لمحول الإشارة التماثلية الى رقمية نوع عداد- منحدر وهو يعتمد على البدء بِعَدّ مناسب, حيث أن المحول نوع عداد – منحدر اعادةً يبدأ بالعَدّ من الرقم صفر (0) في كل عملية تحويل. في هذا العمل, تم اقتراح اربع نقاط لبدء العَدّ وهي : $(00)_H$, $(40)_H$, $(80)_H$ و $(C0)_H$, إذا كانت إشارات الادخال التماثلية ذات المستوى واطئ فإن الدائرة المقترحة سوف تبدأ بالعَدّ $(00)_H$, و للإشارات ذات مستوى أعلى سوف تبدأ من العَدّ $(40)_H$, ولإشارات التحويل بمستوى أعلى أكثر, سوف تبدأ بالعَدّ $(80)_H$ أو العَدّ $(C0)_H$) اعتمادا على مستوى الإشارة التماثلية الداخلة , و هكذا. إن زيادة عدد نقاط بدء العَدّ يؤدي الى زيادة سرعة التغيير أكثر فأكثر , ولكن في الوقت نفسه سوف يزداد عدد دوائر المقارنات التماثلية أكثر فأكثر مما يؤدي الى زيادة تعقيد و كلفة الدائرة المقترحة. في الحقيقة, تم فحص الدائرة المقترحة باختبار 16 و 32 عينة لمستوى فولتية إدخال تماثلية , وقد كانت النتائج مُشجعة حيث أن أقصى زمن للتحويل قد وصل الى 0,64 نانو ثانية, أما في دائرة التحويل نوع عداد – منحدر الاعتيادية قد وصل أقصى زمن التحويل الى 2,65 مايكرو ثانية.

الكلمات المفتاحية: محول D/A ، وقت التحويل ، عداد ثنائي قابل للبرمجة ، منتج العنوان المناسب ، عدد البدء.

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