Design and Implementation of a Microcontroller Based DC/AC Inverter

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Abstract

In this paper, a method is proposed to improve the frequency stability and accuracy of the generated wave in DC/AC square wave inverters using a microcontroller-based stabilized oscillator circuit.

The proposed technique relies on using the 8051 microcontroller as a stable oscillator to generate two anti-phase 50 Hz square waves for the driving power stage of the inverter based on a program stored in its internal ROM. These signals are then boosted to increase their voltage and current levels using BJT switching mode power transistors operating in the push/pull mode. The resulting signal is then raised into the required voltage level with the aid of a step-up transformer.

A practical inverter circuit has been designed and constructed to convert a 12 V battery DC input into 220 V AC output based on the 8051 microcontroller. This circuit consists of an 8051 microcontroller, buffer, driver power transistor stage, final power transistor stage, and a step-up transformer. The inverter circuit has been simulated, implemented, and tested practically. The test measurements have indicated that the circuit gives a full load power of 10 W with full-load voltage regulation of 8%, and a maximum conversion efficiency of 70%.

Keywords: DC/AC Inverter, Power Electronics, 8051 Microcontroller, Square Wave Inverter.

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1. Introduction

An inverter is an electronic circuit that converts direct current (DC) to alternating current (AC) as shown in Figure 1.

Figure 1: Block Diagram of an Inverter.

Inverters are used in a wide range of applications, from small switching power supplies in computers, to large electric utility applications that transport power, especially in renewable energy systems like solar systems, wind power systems, …etc [1]. The inverter is so named because it performs the opposite function of a rectifier. Most inverters do their job by performing two main functions: first they convert the incoming DC into AC, and then they step up the resulting AC to the required voltage level using a transformer. The most important parameters of the inverter circuit are its conversion power efficiency, frequency stability, output voltage regulation, and output waveform distortion [2].

Inverters can be classified into three types according to the shape of the generated waveform as depicted in Figure 2. These are the square wave inverters, modified sine wave inverters, and pure sine wave inverters.

Square wave inverters are simple in design and implementation. The output voltage alternates between positive and negative values. The output waveform, however, has a lot of amount of total harmonic distortion (THD) which results in a considerable power dissipation due to these harmonics. On the other hand, the square wave inverter cannot regulate its AC output voltage when the battery voltage changes significantly. This can cause some types of AC loads to fail suddenly [2].

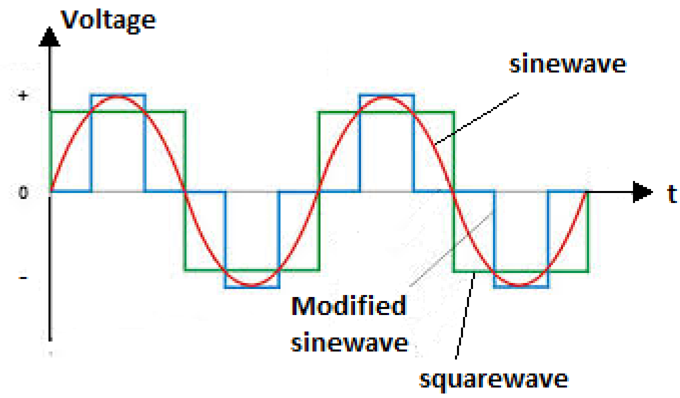


Figure 2: Types of the Generated Inverter Waveforms.

In the modified sine wave inverters, the output signal is similar to a square wave except that it goes to zero for some delay time before switching positively or negatively. This may reduce the THD, and gives better load compatibility. The shape of the waveform can also be controlled to allow regulation of the AC output voltage level as the battery's voltage changes. The pulses of the square wave can be made tall and narrow when the battery voltage is high, and can be made short and wide when the battery voltage is low. This results in a consistent average voltage for supplying the AC loads, and improves load compatibility and performance [3].

Pure sine wave inverters produce a waveform that closely matches the signal of the main power grid system. The generated waveform has very low THD and thus these inverters can run more sensitive AC loads. The design technique of pure sine inverters is complex and usually involves the use of PWM to produce hundreds of positive and negative pulses during each AC cycle. These pulses are then filtered into a smooth sine wave shape. Most true sine wave inverters are able to adjust the duration and timing of each pulse by using a microcontroller or microprocessor control. This allows the voltage and frequency to be controlled to give better load compatibility and performance quality [4, 5].

2. Square Wave DC/AC Inverters

Simple types of square wave inverters consist of a square wave oscillator, driver, power transistor switching circuit, and a transformer as shown in the block diagram of Figure 3.

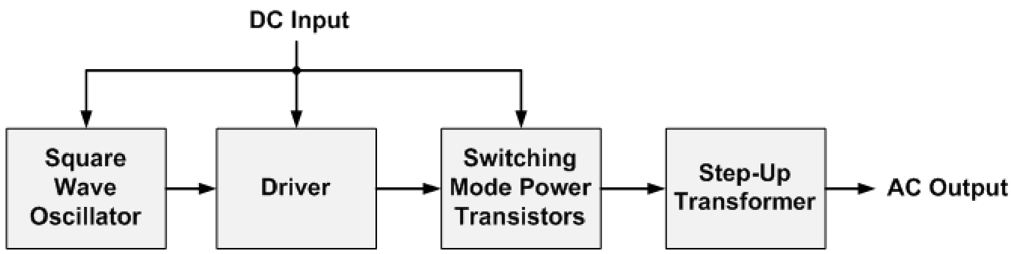


Figure 3: The Main Stages of a Simple Square-Wave DC / AC Inverter.

In this type of DC/AC inverters, the output waveform is not a pure sinusoidal wave but a square alternating wave. This means that the output signal contains a significant amount of harmonics accompanying the fundamental component. The square wave oscillator is a multivibrator circuit providing a square wave with a low frequency of 50 Hz. This circuit can use the NE555 or a similar timer to produce the required signal. The generated signal is then applied to a power transistor driving circuit in order to increase its current level. This stage is an intermediate one that drives another higher power stage. The transistors at the final power stage operate in a switching mode with a high current rating for high efficiency. The signal is then converted to 220 V level by means of a step-up transformer.

3. The Proposed Inverter Circuit

Figure 4 presents a generalized diagram for the proposed inverter. To simplify the analysis of the circuit, one can divide it into several stages and deal with each stage independently.

This circuit uses BJT transistors as switching devices and a center-tap step-up transformer to convert a 12 V DC input into a 220 V AC output. The output waveform of this circuit is a square wave, and the power output depends on the transformer power rating, in addition to the current rating of the power transistors.

The 8051 microcontroller is used as a stabilized oscillator to generate a low frequency square wave that can be applied to the driving stage power transistors via a tri-state buffer. This buffer is used to isolate the microcontroller port from the power stage, as well as to provide the driving power stage with adequate base currents to switch-on the transistors. The microcontroller is used to increase the frequency stability of the generated waveform, and to get butter accuracy of the generated frequency. This can be accomplished using the program stored in the on-chip ROM of the microcontroller. Both of the microcontroller and buffer chips need a regulated 5 V voltage which can be obtained from an IC voltage regulator.

The current level of the generated square wave is increased by the driving power transistors, and the final power stage. The step-up transformer can thereafter raise the amplitude of the generated waveform into the required voltage level.

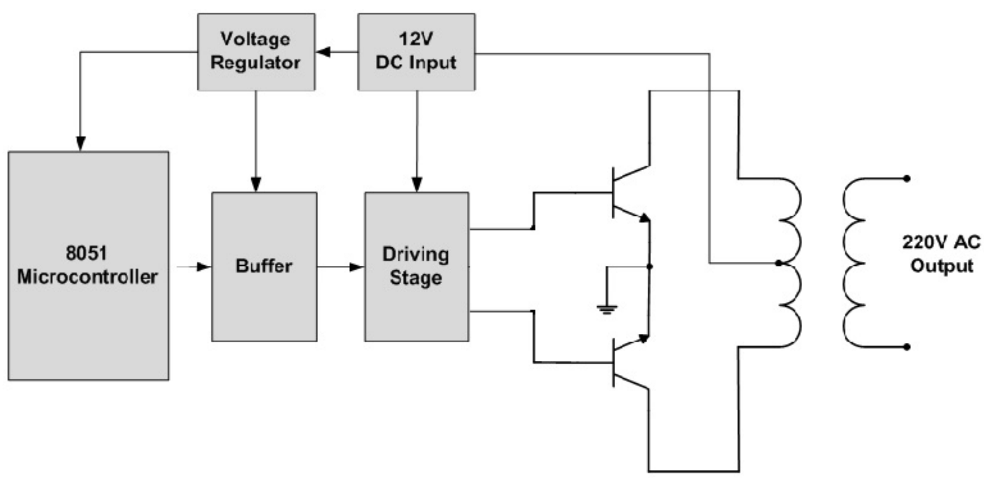


Figure 4: Overall Block Diagram of the Proposed DC/AC Inverter.

4. Inverter Design

In this section, the design approach of the practical inverter circuit will be clarified and illustrated. The design process involves designing the microcontroller circuit to operate as a 50 Hz square wave oscillator, designing the driver and power stage, selecting the step-up transformer, and finally assembling the overall circuit.

4.1 Designing the 8051 Microcontroller-Based Oscillator Circuit

The purpose of the oscillator circuit is to provide a clean square wave with an ideal frequency of 50 Hz, which is the frequency of the required AC voltage.

In order to generate a stabilized low frequency signal, it is preferred to produce first a high frequency signal from a crystal oscillator, and then use frequency dividers to obtain the required low frequency. This technique can be realized in software by programming a microcontroller to generate the required square waves with a pre-determined time delays.

The Atmel 89C51 microcontroller chip has been selected for this design. This is a special IC of the 8051 family. It is a low cost 8-bit microcontroller with an internal Flash ROM code memory of 4 KB, and an internal RAM of 128 B. It possesses 4 I/O ports, each containing 8 lines and has also two 16-bit internal timers and one serial port.

The timers of the 8051 microcontroller are referred as Timer 0 and Timer 1. They can be used as either timers or counters. Each 16-bit timer is implemented by two 8-bit registers as low byte and high byte. For timer 0, the low byte is referred as TL0, while the high byte is referred as TH0. For Timer 1, the equivalent registers are TL1 and TH1 respectively. Each timer can operate in four different modes depending on the codeword saved in a specialized register called TMOD. In mode 1, the operation is 16-bit timer/counter with the TH and TL registers are cascaded. Each timer needs a clock pulse to start. The clock frequency for the timers of the 8051 equals the crystal frequency divided by 12 [6]. For example, if the crystal frequency is 10 MHz, then the clock frequency will be 833.333 kHz, and the clock interval will thus equal to 1.2 μs.

The starting and stopping process of the timers can be controlled via software by setting and clearing a special flag bit, called TR (timer start), respectively. Before starting the timer, registers TL and TH should be loaded with certain initial values. The 16-bit timer can be loaded with values ranging from 0000H up to FFFFH. After loading the timer, it starts to count up starting from the initial preset value. When the timer reaches its maximum allowable value (FFFFH), it overflows and resets to 0. This condition can be monitored through a special flag bit, called TF (timer flag). When the timer overflows, TF becomes 1. When the timer flag is raised, the timer can be stopped by clearing the TR bit. In order to repeat the counting process, the registers TH and TL must be reloaded with the original value, and the TF flag must be reset to 0.

To use the 8051 microcontroller as a square wave generator, the time delays of the HIGH and LOW intervals for the square wave should be determined exactly to find the number of required counts of the timer. The decimal value that should be loaded into the TL and TH registers for a specified delay time t_d can be calculated from [6]:

$$N = (N_{\max} + 1) - \frac{t_d}{T_{ck}} \tag{1}$$

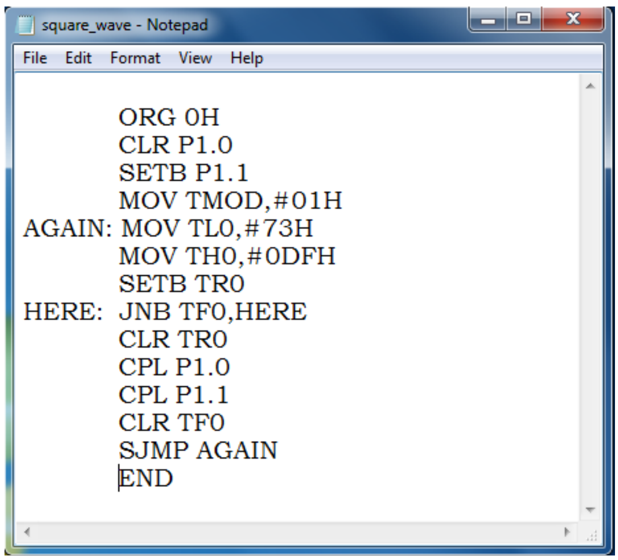
Where N_{max} is the full-scale value of the timer which equals to 65535 (FFFFH), and T_{ck} is the clock period and is equal to the reciprocal of the clock frequency f_{ck}.

The value of N can be converted from decimal to hexadecimal before loading it into the timer registers. Thus, to generate a square wave of 50 Hz, a time delay of 10 ms should be produced for each of the HIGH and LOW portions of the signal. A 10 MHz crystal is used for the AT89C51 microcontroller, which ensures an internal clock frequency of 833.333 kHz, and a clock interval T_{ck} of 1.2 µs. Substituting both t_d = 10 ms, and T_{ck} = 1.2 µs in equation (1) yields N = 57203. This value is equivalent to DF73H. Figure 5 presents the 8051 assembly code for generating two out-of-phase 50 Hz square-wave signals at pins P1.0 and P1.1 of the AT89C51 microcontroller.

The program resides in the microcontroller's on-chip memory at a starting address of 00H. Initially, pin P1.0 of Port 1 is cleared, and pin P1.1 is set to 1 to generate 180^o out of phase signals. Timer 0 of the 8051 chip is selected by properly defining the codeword in the TMOD control register (in this case codeword = 01H). The calculated hexadecimal value (DF73H) is loaded into the TL0 and TH0 registers of timer 0. Afterwards, the timer is started counting by activating the TR0 flag bit through the SETB instruction. The state of the TF bit (timer flag) is monitored using the JNB instruction. Actually, the timer will count a total number of clock signals equal to 208DH (FFFFH-DF73H+1) before reaching the overflow state. When the timer reaches its maximum limit, the TF bit will go HIGH and the counting process is stopped by resetting the flag bit TR0 to 0. Before repeating the counting cycle, both signals at pin P1.0 and P1.1 should be complemented using the CPL instruction and timer flag TF should be cleared. This process is repeated continuously to obtain two anti-phase 50% duty cycle pulse signals.

The assembly program has been converted to hex file using the MIDE-51 assembler, and then burned into the flash memory of the microcontroller using a commercial universal programmer.

Figure 6 shows the schematic diagram of the AT89C51 microcontroller to generate the 50 Hz square wave signals. The 74LS244 tri-state buffer is connected to Port 1 of the microcontroller in order to isolate it from the power stage, and to provide the power transistors with the necessary current for driving them.




```
        ORG 0H
        CLR P1.0
        SETB P1.1
        MOV TMOD,#01H
AGAIN:  MOV TL0,#73H
        MOV TH0,#0DFH
        SETB TR0
HERE:   JNB TF0,HERE
        CLR TR0
        CPL P1.0
        CPL P1.1
        CLR TF0
        SJMP AGAIN
        END
```

Figure 5: The Assembly Program Used to Generate the 50 Hz Signals.

4.2 Designing the Power Stage

The second stage in the inverter design is to synthesize the transistor power circuit in order to increase the current and voltage levels of the generated square waves. This circuit consists of two pairs of transistors connected in Darlington configuration in order to increase the current gain [7]. This circuit actually operates in the push/pull mode. Figure 7 shows a schematic diagram of the circuit.

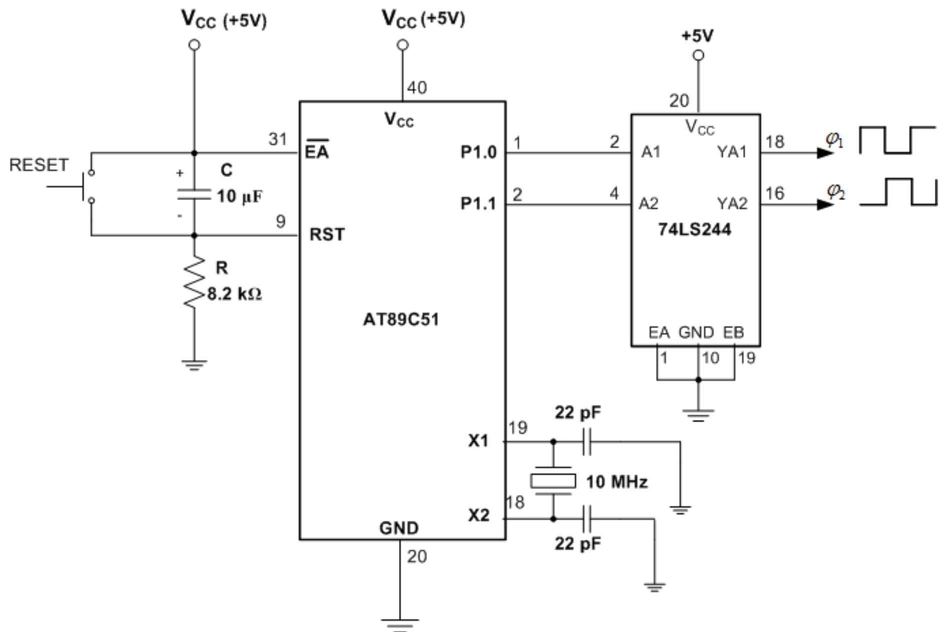


Figure 6: Schematic Diagram of the Microcontroller-Based Oscillator.

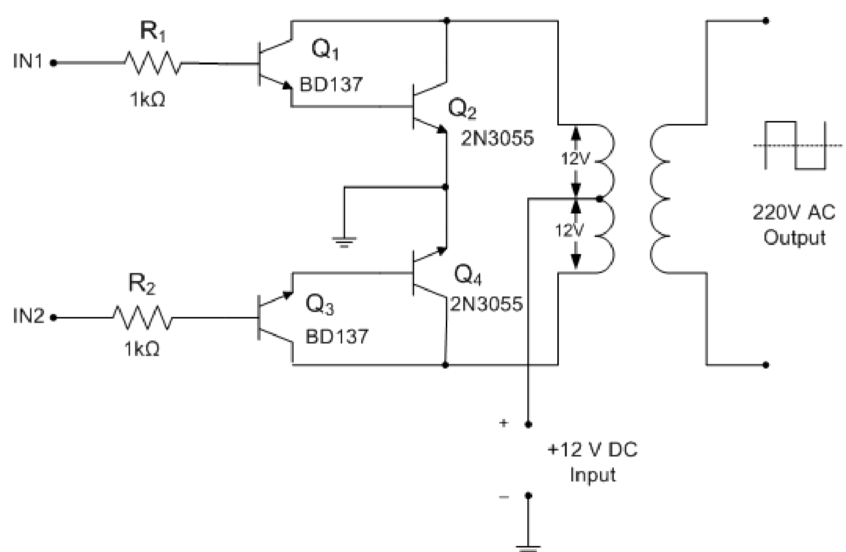


Figure 7: Schematic Diagram of the Power Stage.

Resistors R_1 and R_2 are used to control the input base currents of Q_1 and Q_3. They can be chosen to place the transistors in saturation when conducting. This will minimize the losses due to transistors' power dissipation. For a specified collector current in Q_2 or Q_4, resistor R_1 should be chosen such that [7]:

$$R_1 \leq \frac{V_{IN1} - V_{BE1(sat)} - V_{BE2(sat)}}{I_{C2} / (h_{FE1} . h_{FE2})} \tag{2}$$

Where V_{IN1} is the peak input voltage at the base of Q_1 when conducting and is equal to 5 V, I_{C2} is the collector current of Q_2, while h_{FE1} and h_{FE2} are the minimum values of the DC current gain for Q_1 and Q_2 respectively. For a collector current passing in Q_2 of 1A, h_{FE1} = 40, h_{FE2} = 20, and $V_{BE1(sat)} = V_{BE2(sat)}$ = 0.75V, then R_1 should be less than 2.8 kΩ. A value of 1 kΩ was selected to place the transistors deeply in saturation. The value of resistor R_2 is calculated in a similar manner as Q_3 and Q_4 are identical with Q_1 and Q_2 respectively.

Q_1 is working as a driver transistor for Q_2, and Q_3 is the driving stage of Q_4. Without these driving transistors, the input signals would not drive Q_2 and Q_4. Q_1 and Q_3 are medium power transistors, while Q_2 and Q_4 are high power transistors. The power transistor BD137 has been chosen to implement Q_1 and Q_3. This is a medium power transistor with maximum current rating of 1.5 A. On the other hand, the well–known power transistor 2N3055 has been selected to implement Q_2 and Q_4. This transistor can pass a maximum collector current of 15 A.

During the first half interval of the square wave (ON period), both Q_1 and Q_2 will conduct (becoming ON), while Q_3 and Q_4 will be OFF. On the other hand, during the second half of the interval of the square wave, both Q_3 and Q_4 will be ON while Q_1 and Q_2 will be OFF. So, the current will reverse its direction through the primary winding of the transformer during each half cycle, thereby producing an AC alternating signal. The signal amplitude will then be stepped up to 220 V at the secondary winding. Actually, a center–tap step-up transformer (12 V to 220 V) with a maximum current rating of 1 A at the low voltage side has been used in this design.

The power stage of the inverter circuit has been simulated using a powerful circuit simulator (*ADS* of Agilent Technologies) to scope the voltage waveforms at the base and collector of the power transistors as well as the output voltage and load current. Other popular circuit simulators, such as *PSpice*, can also be used for such a purpose [8]. The input driving signals of the circuit are provided from two out-of-phase pulse generators with a frequency of 50 Hz and amplitude of 5 V. The simulation has been carried out for a load power of 10 W.

Figure 8 shows the base voltages of Q_1 and Q_3. The amplitude of the base voltage of Q_1 reaches approximately 1.4 V which equals approximately $V_{BE1(sat)}$ plus $V_{BE2(sat)}$. The spikes appearing in the transitions of the signals are due to the emitter-base junction capacitance. These spikes can be eliminated practically using freewheeling diodes. It is clear that these waveforms are out of phase to prevent Q_1 and Q_3 from conduction at the same time, which is necessary for the push-pull operation.

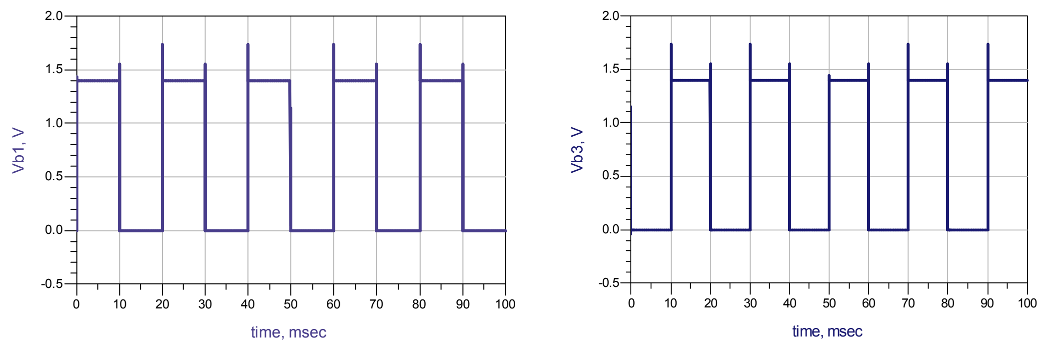


Figure 8: Simulated Base voltages of Q_1 and Q_3.

In Figure 9 the collector to emitter voltage of Q_2 is presented. As shown from this plot, the collector signal of Q_2 swings between $V_{CE(sat)}$ and $2V_{dc} - V_{CE(sat)}$, where V_{dc} is the inverter input DC voltage. The saturation voltages of Q_2 and Q_4 are relatively high and increase with collector current. The voltage at each half of the primary winding of the center-tapped transformer is found from:

$$v_{pr}(t) = V_{dc} - v_{CE}(t) \tag{3}$$

The primary voltage v_{pr} is sketched in Figure 10, with a positive peak value of $V_{dc} - V_{CE(sat)}$ and a negative peak value of $-V_{dc}+V_{CE(sat)}$.

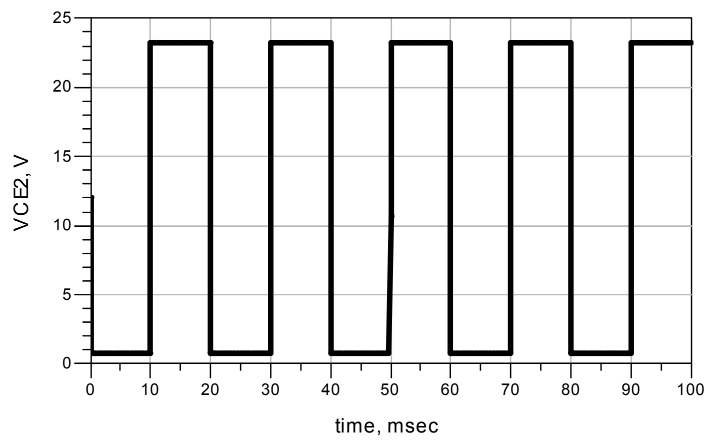


Figure 9: Simulated Collector-to-Emitter Voltage of Q_2.

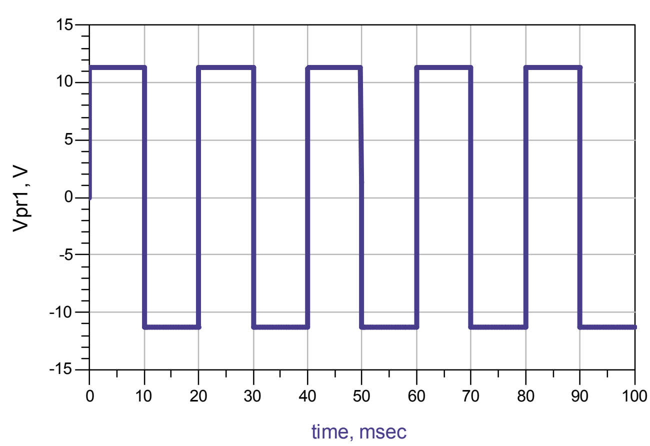


Figure 10: Simulated Waveform at the Primary Winding of the Transformer.

The output signal of the inverter is sketched in Figure 11. For a load of 10 W, the simulated peak value is about 208 V. It is well-known that the r.m.s value of the voltage equals the peak value for the square wave.

Figure 12 displays the spectrum of the output voltage up to the 10th harmonic component. As shown from Figure 12, the third harmonic is the closest component to the fundamental signal. The output signal has no DC component. Finally, Figure 13 shows the output current signal.

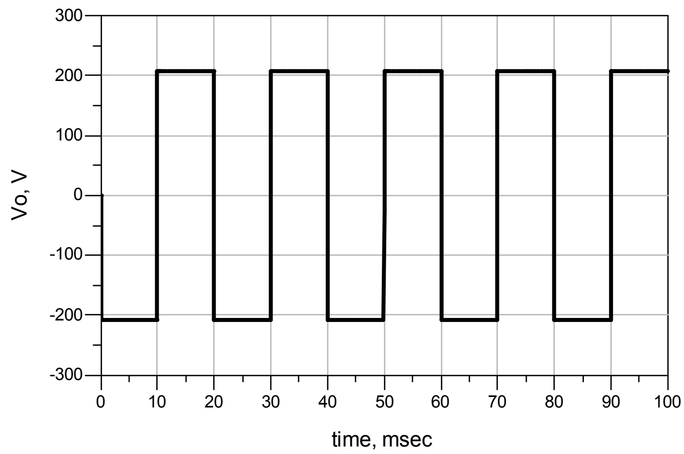


Figure 11: The Simulated Output Signal of the Inverter.

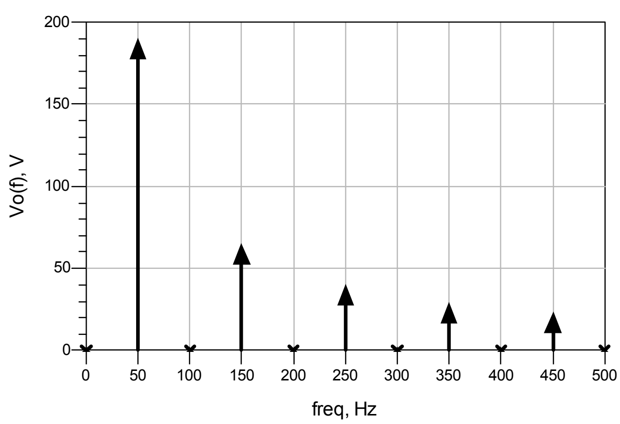


Figure 12: Output Voltage Spectrum.

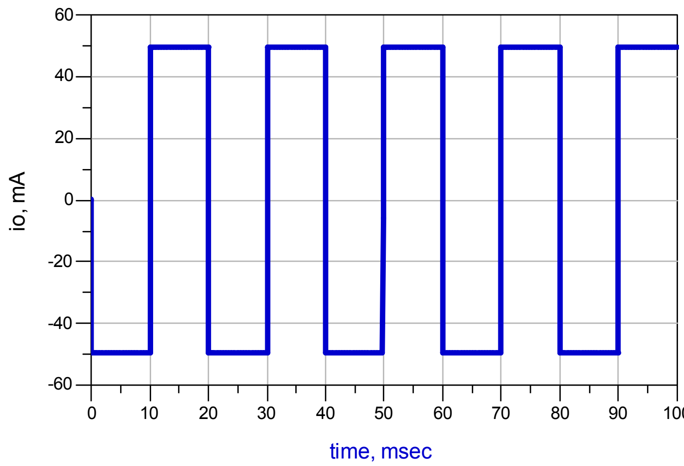


Figure 13: Simulated Load Current.

5. Circuit Construction and Testing

Figure 14 shows the schematic diagram of the final inverter circuit. The 5V DC input voltage of the AT89C51 microcontroller and the 74LS244 buffer is obtained from a 7805 IC regulator that has been connected to the 12V DC input as shown in Figure 14.This regulator can be used to provide a constant 5V DC voltage for the TTL or CMOS digital ICs for stable operation. Two fast switching diodes, D_1 and D_2, are connected at the bases of Q_1 and Q_3 to remove the negative spikes of the base signals which may otherwise damage the emitter-base junctions of the transistors.

The inverter circuit was implemented on a test breadboard, and all the power transistors were fixed on suitable heat sinks. Figure 15 depicts a photograph of the assembled circuit. As illustrated in Figure 15, the DC input voltage is taken from a 12V DC battery of high capacity. In Figure 16, the square waves generated by the 8051 microcontroller at pins P1.0 and P1.1 are displayed on a digital storage oscilloscope. As shown from this figure, the generated signals are clean with constant amplitude of 5 V. The measured stabilized frequency is 49.75 Hz as depicted in Figure17.

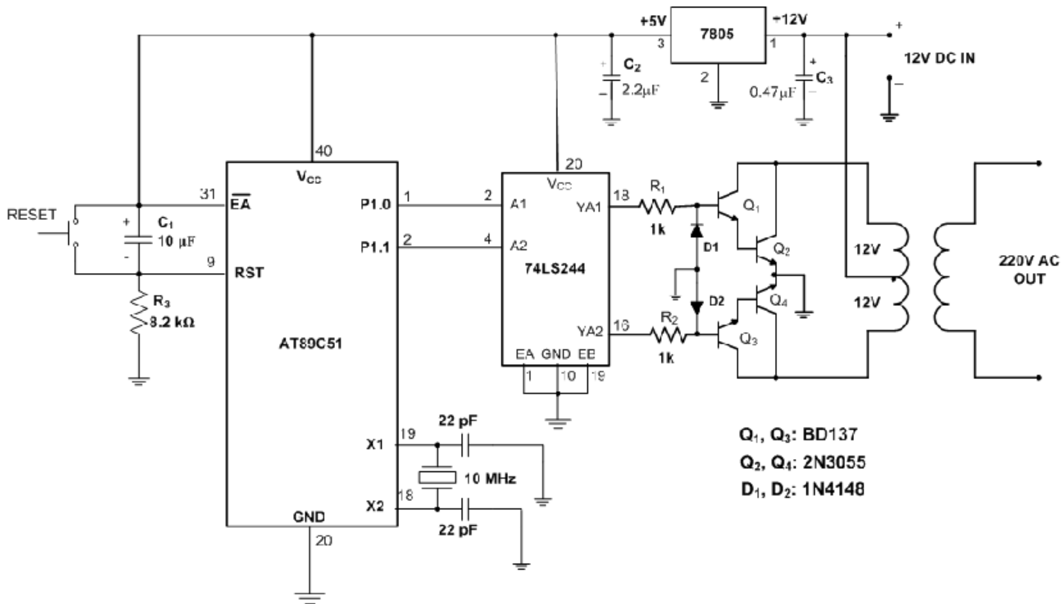


Figure 14: Schematic Diagram of the Inverter Circuit.

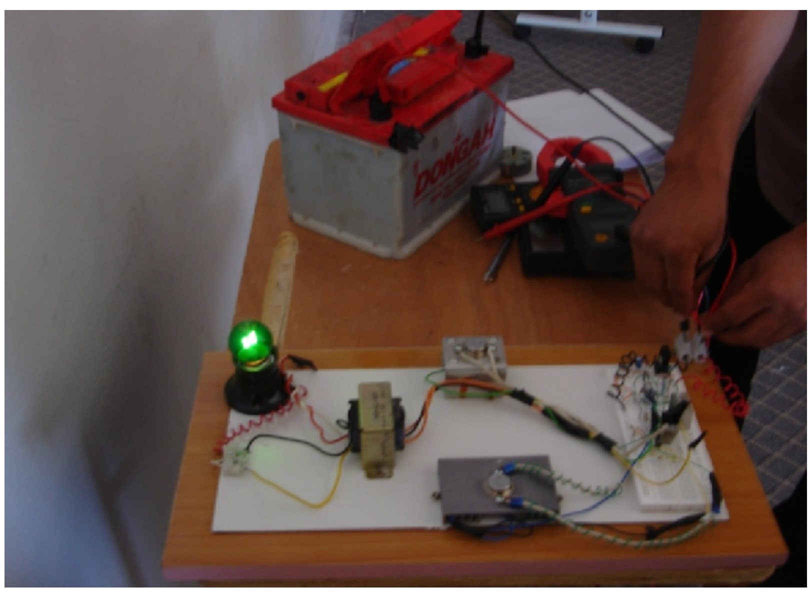


Figure 15: The Implemented Inverter Circuit.

Figure 16: Microcontroller Generated Square Waves Displayed on the Oscilloscope (Scale : 5 V/div, 10 ms/div).

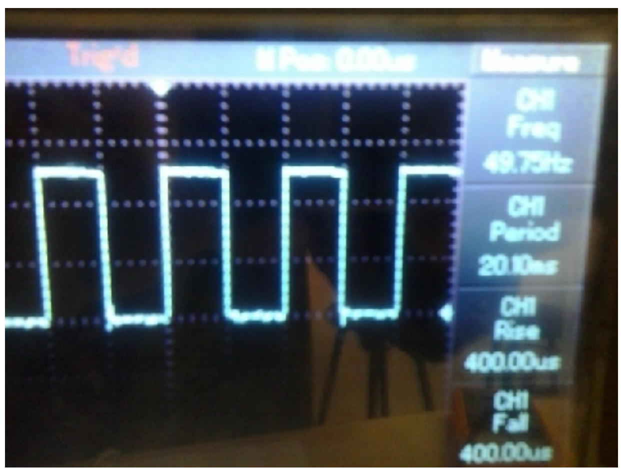


Figure 17: Signal at the Output of the 74LS244 Buffer (Scale: 2V/div, 10 ms/div)

The signal at the base of transistor Q_1 is displayed in Figure 18, while Figure 19 presents the signal at the collector of transistor Q_2 at full-load. The distortion in these signals is referred to the nonlinear operation of the power transistors and their non-ideal switching characteristics.

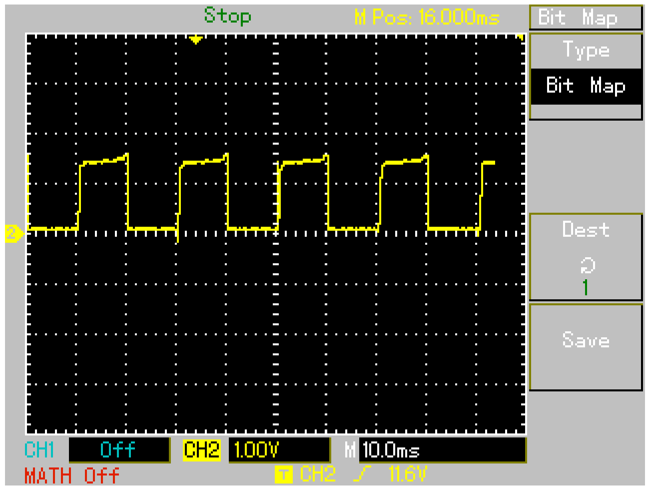


Figure 18: Signal at the Base of Transistor Q_1

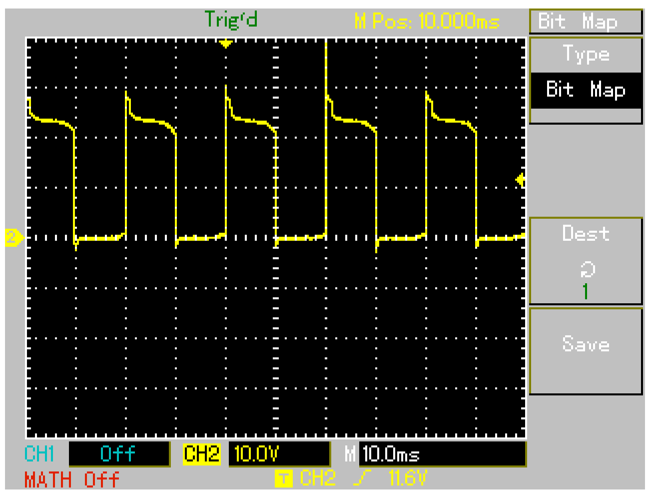


Figure 19: Signal at the Collector of Transistor Q_2

The performance evaluation results were obtained through the experimental test setup shown in Figure 20.

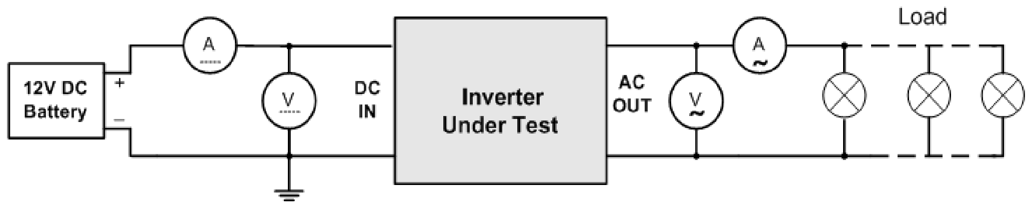


Figure 20: Practical Test Setup for the Designed Inverter.

In this test setup, a 12 V car battery was used for DC input and 220 V, 2 W bulbs (lamps) were used for the AC load. The input voltage, input current, output current, and output voltage have been measured while changing the wattage of the load bulbs. The output voltage actually falls with a heavy load. The consumption of power by the bulbs changes with the voltage.

Figure 21 shows a sketch of the output voltage versus load power, while Figure 22 shows a sketch of the inverter efficiency versus load power where:

$$\eta = \frac{P_{out}}{P_{in}} \times 100 = \frac{V_{out}.I_{out}}{V_{dc}.I_{dc}} \times 100 \qquad (4)$$

Where V_{dc} and I_{dc} are the DC input voltage and current respectively, and V_{out} and I_{out} are the r.m.s voltage and current at the output.

It can be seen from Figure 21 that the output voltage falls with increasing load power and reaches to 200 V approximately at 10 W output (Full-load). From this figure, the AC voltage regulation can be calculated as:

$$VR = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 \qquad (5)$$

$$= \frac{216 - 200}{200} = 8\%$$

Where V_{NL} is the no-load output voltage and V_{FL} is the full-load output voltage.

On the other hand, the efficiency increases with the increase in load power and reaches a maximum value of 70% approximately at 10 W load power as shown in Figure 22.

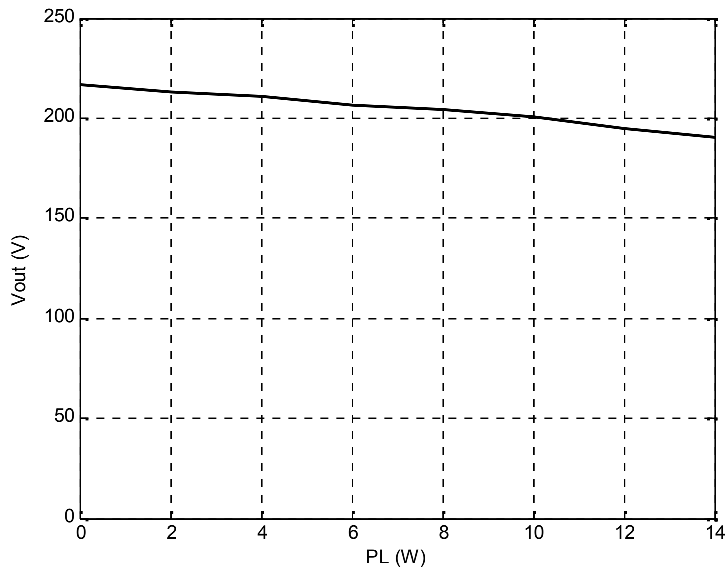


Figure 21: Output Voltage versus Load Power

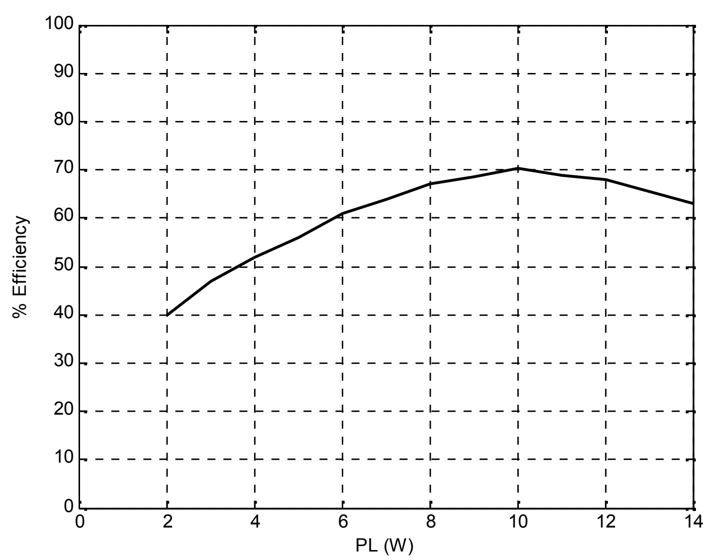


Figure 22: Conversion Efficiency versus Load Power

6. Summary and Results Discussion

In this work, a practical inverter circuit to convert a 12 V input DC voltage into 220 V AC output voltage has been designed and constructed based on the 8051 microcontroller.

After reporting the test results, it has been shown that the stability and accuracy of the frequency for the generated waveform are greatly enhanced through the use of the microcontroller as a stabilized oscillator. It was also noticed that the output voltage falls from 216 V at no-load to approximately 200 V at full-load with an overall voltage regulation of 8%. The main cause in load voltage reduction is the limited power capability of the transformer, and the harmonics presented in the output waveform. The inverter efficiency increases with the load power reaching to 70% at 10 W. Factors affecting the overall conversion efficiency include power dissipation in the power transistors, transformer leakage and core loss, and power consumption in the voltage regulator module and the microcontroller chip. The relatively high saturation voltage of the 2N3055 power transistor reduces the effective amplitude of the generated signal.

The current rating of the transformer is 1 A, and a larger transformer can be used to obtain much more load power. The amplitude regulation of the inverter can be improved by using a 12V IC voltage regulator for the power transistors with high current capability. This will, however, increase the power losses and hence degrade the conversion efficiency. Power MOSFETs can be used as the switching devices instead of the BJTs to minimize the switching losses.

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تصميم وتنفيذ عاكس تيار مستمر/ تيار متناوب باستخدام المسيطر الدقيق

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المستخلص

في هذا البحث تم اقتراح طريقة لتحسين الإستقرارية الترددية ودقة تردد الإشارة المتولدة لدوائر العاكس ذات الإشارة المربعة عن طريق استخدام دائرة مذبذب عالي الاستقرار مبنية باستخدام المسيطر الدقيق.

تعتمد التقنية المقترحة على استخدام المسيطر الدقيق 8051 ليعمل كمذبذب عالي الاستقرار لتوليد إشارتين مربعتين متعاكستين بالطور بتردد 50 Hz وإرسالهما إلى مرحلة مشغل القدرة لدائرة العاكس عن طريق برنامج مخزون في ذاكرته الداخلية الدائمية. يتم بعد ذلك تضخيم هذه الإشارات لزيادة مستوى التيار والفولتية فيها عن طريق مضخم قدرة تحويلي يعمل بطريقة الدفع/السحب بترانزستورات قدرة من نوع BJT. ويتم رفع جهد الإشارة المتناوبة المتولدة الى القيمة المطلوبة بواسطة محول رافع للجهد.

تم تصميم وتنفيذ دائرة عاكس عملية لتحويل جهد مستمر مقداره 12 V إلى جهد متناوب قيمته الفعالة 220 V باستخدام المسيطر الدقيق 8051. تتكون الدائرة المقترحة من المسيطر الدقيق 8051 وعازل ومضخم قدرة أولي ومرحلة تضخيم قدرة نهائية بالإضافة إلى محول رافع للجهد. تمت محاكاة دائرة العاكس بواسطة الحاسوب ومن ثم تنفيذها واختبارها عملياً. وقد بينت نتائج القياسات العملية بأن الدائرة تعطي قدرة خرج مقدارها 10 W للحمل الكامل بتنظيم جهد مقداره 8% وبكفاءة تحويل قصوى تصل إلى 70%.

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